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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/788,492 | 03/01/2004 | Nobuaki Hashimoto | 118876 | 9029 |

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| EXAMINER | |
|---|---|
| RICHARDS, N DREW | |
| ART UNIT | PAPER NUMBER |
| 2815 | |

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/788,492 | HASHIMOTO, NOBUAKI | |
| | Examiner | Art Unit | |
| | N. Drew Richards | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/1/04, 9/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Information Disclosure Statement*

1. The citation of attorney docket numbers in the IDS filed 3/1/04 is an improper citation. The examiner has crossed through these citations. However, the applications referred to by these citations have been considered by the examiner and are cited on the attached PTO-892 by their application number.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 8, 11, 14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 01-164044 (cited in IDS filed 9/28/05).

With regard to claim 1, JP 01-164044 teaches an electronic device in figure 3 comprising:

- a substrate 1 on which an interconnect pattern 2 is formed;
- a chip component 4 having a first surface (top surface) and a second surface (bottom surface) opposite to the first surface, the chip component 4 being mounted in such a manner that the second surface faces the substrate 1;
- a metal layer 4a formed on the first surface of the chip component;
- an insulating section 6 formed adjacent to the chip component 4; and

- an interconnect 7 which is formed to extend from above the metal alyer 4a, over the insulating section 6 and to above the interconnect pattern 2.

JP 01-164044 does not explicitly teach a pad formed on the first surface of the substrate, the pad being more oxidizable than the metal layer. However, this limitation is considered obvious to one of ordinary skill in the art in view of JP 01-164044. One of ordinary skill in the art would recognize that the metal layer 4a is connected to metal lines within the chip component in order to allow electrical connection and communication with devices formed in the chip and that the metal lines would include a pad for external connection. It would have been obvious to one of ordinary skill in the art to form the pad from a highly conductive metal such as aluminum in order to allow low resistance, high speed electrical connections and signals within the chip. Thus, it would have been obvious to one of ordinary skill in the art to form a pad below the metal layer where the pad is more oxidizable than the metal layer.

With regard to claim 2, the insulating section is formed of resin.

With regard to claims 3 and 4, the insulating section has an inclined surface descending in an outward direction from the chip component.

With regard to claim 5, JP 01-164044 performs the claimed "mounting" and "forming" steps as claimed to arrive at the same device of claim 1. Including the pad of an oxidizable metal is obvious as discussed with regard to claim 1.

With regard to claim 8, the insulating section is formed of resin.

With regard to claims 11 and 14, the insulating section has an inclined surface descending in an outward direction from the chip component.

With regard to claim 17, JP 01-164044 teaches a circuit board 1 on which the device of claim 1 is mounted. For arguments sake, if claim 17 requires a further circuit board on which the device including substrate 1 of JP 01-164044 is mounted, this claim is still considered obvious as it would have been obvious to one of ordinary skill in the art at the time of the invention to mount the device of JP 01-164044 on a printed circuit board in order to integrate the devices formed therein with other devices, such as mounting the chip on the mother board of a computer.

With regard to claim 18, the device of JP 01-164044 is considered an electronic instrument.

4. Claims 6, 7, 9, 10, 12, 13, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 01-164044 as applied to claims 1-5, 8, 11, 14, 17 and 18 above, and further in view of Ito et al. (US Patent No. 6,625,032 B1).

With regard to claims 6 and 7, JP 01-164044 does not explicitly teach the interconnect being formed of a dispersant including electrically conductive particles or forming the layer includes ejecting the material over the metal layer, the insulating section, and the interconnect pattern.

Ito et al. teach on column 1 lines 30-37 that a dispersant including electrically conductive particles is ejected onto a substrate to form conductive layers. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the prior art conductive particles in dispersant ejecting method of Ito et al. in the method of JP 01-164044 to obtain rapid implementation of interconnects on surfaces.

With regard to claims 9 and 10, JP 01-164044 teach the insulating section formed of resin.

With regard to claims 12, 13, 15 and 16, JP 01-164044 teach the insulating section has an inclined surface descending in an outward direction from the chip component.

### *Double Patenting*

5. Claims 1-18 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-34 of copending Application No. 10/788449 in view of JP 01-164044. Claims 1-34 contain all the limitations of claims 1-18 except for a metal layer on the pad where the metal layer is less oxidizable than the pad, and the insulating section having an inclined surface. However, these limitations are obvious in view of JP 01-164044 which teaches gold for the a land part to ensure reliability of electrical connections and an incline in the resin insulator to allow for a plane with no steep stepped part so that a low cost interconnection method such as screen printing can be used.

This is a provisional obviousness-type double patenting rejection.

### *Conclusion*

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Application 10/788447, U.S. Application 10/788295,

Kunitomo et al. (US Patent 5550408), Nakayama et al. (US Patent 6621172 B2), Gleason et al. (US Patent No. 6825564 B2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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